INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920030122US1	10/707,286 ~~Not Yet Assigned~~
Applicant(s) Ditlow et al.	
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*EXAMINER INITIAL	OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*
VS	"An Analytical Approach to Floorplanning for Hierarchical Building Blocks Layout", IBM Technical Disclosure Bulletin, Vol. 33, No. 6A, Nov. 1990, pp. 164-165.
VS	Ying et al., "An Analystical Approach to Floorplanning for Hierarchical Building Blocks Layout", IEEE Transactions on Computer-Aided Design", Vol. 8, No. 4, April 1989, pp. 403-412.
VS	Yamada et al., "A Block Placement Method Based on Balloon Model", IEEE International Sympsosium on Circuits and Systems, Vol. 3, 1990, 1680-1683.
VS	G. Vijayan, "Overlap Elimination in Floorplans",Proceedings Fourth CSI/IEEE International Symposium on VLSI Design, 1991, PP. 157-162.
VS	Choi et al.,"A Floorplanning Algorithm Using Rectangular Voronoi Diagram and Force-Directed Block Shaping", International Conference on Computer-Aided Design, Nov. 1991, pp. 56-59.

EXAMINER	DATE CONSIDERED
VUTHE SIEK	7/28/05

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.